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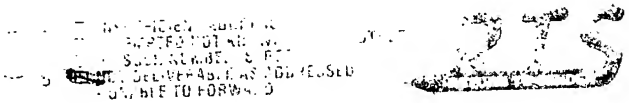

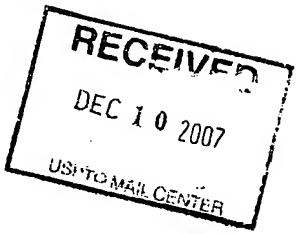

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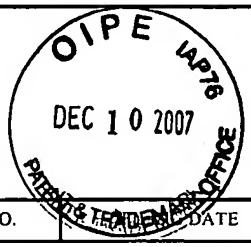

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APPLICATION NO.	FILING OR 371(C) DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,320	01/29/2004	Marcelo Krygier	P-6505-US	1221

27130 7590 11/28/2007

EITAN, PEARL, LATZER & COHEN ZEDEK LLP
10 ROCKEFELLER PLAZA, SUITE 1001
NEW YORK, NY 10020

EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

MAIL DATE	DELIVERY MODE
11/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,320	KRYGIER, MARCELO	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11 and 12* is/are allowed.

6)☒ Claim(s) *1-10 and 13-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-17 have been presented for examination in this application. In response to the last office action, claims 18-24 have been added. As the result, claims 1-24 are pending in this application.

The applicant's remarks and amendment to the claims have been considered with the results that follow,

Claims 11-12 are allowed

Claims 1-10,13-24 are rejected.

All rejections and objections not explicitly repeated below are withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

A person shall be entitled to a patent unless -

(a) the invention was known or used by other's in this country or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another fled in the United States before the invention thereof by the applicant for patent, or on an international application by another

who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-8,13-18 are rejected under 35 U.S.C. 102 (a) as being anticipated by Lakhani et al (US 2003/0126385).

As in claim 1, Lakhani discloses a method for operating a non-volatile memory device comprising: using the one or more unused bits of the address argument (Lakhani's page 7 table A, c1, c2 bits) of the command as an addressing mode field (Lakhani's paragraph 84 discloses a method for operating non-volatile devices using bits C1, C2 that is not being used as addressing bits) to determine whether said address argument is a byte address argument or a block address argument (Lakhani's page 7 table A, paragraph 75 discloses C1,C2 bits being used to determine the first mode, address bits being interpreted as byte address for an operation in a memory device, see paragraph 69; Lakhani's paragraph 76 discloses C1,C2 bits being used to determine the second mode, corresponding to the claim's block mode, in which an operation occurs for data in blocks of memory devices, see paragraph 70).

Lakhani further discloses receiving a command that includes an address argument comprising a plurality of address bits, one or more of address bits comprising unused bits and any remaining bits providing an address for a location in the non-volatile memory device (Lakhani's control bits and address bits corresponds to the claim's address argument. Because the control bits do not contain address bits of memory device such as bits A [22:0] etc..therefore the control bits are unused bits of an address argument as claimed. Lakhani further discloses the control bits are used as addressing mode (as claimed) to indicate the address is for byte mode addressing or block mode addressing (as claimed, see above paragraph));

Lakhani further discloses the remaining bits provide a byte address when the address argument is a byte address argument and the remaining bits provide a block address when the address argument is a block address argument (Lakhami's paragraphs 70,76 remaining bits such as a[22:0],E[7:0] etc.. provide an address for corresponding addressing modes).

As in claims 2-3, Lakhani discloses determining that the address argument is the byte address argument when the addressing mode field is zero (claim 2; Lakhani's paragraph 75 discloses the C1, C2 having value 0 for first mode/byte mode operation); determining that the address argument is the block address argument when the addressing mode field is one (claim 3; Lakhani's paragraph 76 discloses C1 having value of 1 for second mode/block mode operation).

As in claims 4-5, Lakhani discloses accessing a byte address within a memory unit according to the byte address argument if said address argument is a byte address argument (claim 4); accessing a block address within a memory unit according to the block address argument if said address argument is a block address argument (claim 5). The claims rejected based on the same rationale as of claims 1 and 2. Lakhani's paragraph 84 discloses a method for operating non-volatile devices using bits C1, C2 that is not being used as addressing bits.

As in claims 6-7, Lakhani discloses wherein using said one or more unused bits comprises using a least significant bit of said address argument (claim 6); wherein using said one or more unused bits comprises using a most significant bit of said address argument (claim 7). Lakhani's table 1, paragraph 75 discloses using the C1, C2 bits comprising using the associating address bits to address particular cells in the memory devices. The address bits include both most significant and least significant bits.

As in claim 8, Lakhani discloses an apparatus comprising: a non volatile memory unit (Lakhani's Fig 2: #16 , paragraph 13), a controller adapted to determine whether an addressing mode to access said memory unit is a byte addressing mode or a block addressing mode and to send a command to access data within said memory unit according to said addressing mode (Lakhani's Fig 2, associating controlling logic such as controller engine #41, predecoder #50), wherein: in the byte addressing mode, address bits of an address argument of the command provide a byte address, and in the block addressing mode, said address bits of the address argument of the command provide a block address (Lakhami's paragraphs 70,76 bits such as a[22:0],E[7:0] etc.. provide an address for corresponding addressing modes).

As in claim 13, Lakhami discloses a storage medium having stored thereon instructions that when executed by a computing platform functionally associated with a non-volatile memory device result in (Lakami Fig 2: #16 non volatile memory of a flash memory system, paragraphs 5,17 providing instructions for a standard operating system being executed by a computing platform/host processor that result in) using one or more bits of a command as an addressing mode field to determine whether an address argument of the command is a byte address argument or a block address argument (Lakhani's page 7 table A, paragraph 75 discloses C1,C2 bits being used to determine the first mode, address bits being interpreted as byte address for an operation in a memory device, see paragraph 69; Lakhani's paragraph 76 discloses C1,C2 bits being used to determine the second mode, corresponding to the claim's block mode, in which an operation occurs for data in blocks of memory devices, see paragraph 70), wherein: when said address argument is a byte address argument, address bits of the address argument provide a byte address, and when said address argument is a block address argument, said address bits of the

address argument provide a block address (Lakhami's paragraphs 70,76 bits such as a[22:0],E[7:0] etc.. provide an address for corresponding addressing modes).

As in claim 14, Lakhani discloses using one or more unused bits of the address argument as the addressing mode field. Lakhani's paragraph 84 discloses a method for operating non-volatile devices using bits C1, C2 that is not being used as addressing bits.

Claim 15 rejected based on the same rationale as of claim 2.

Claim 16 rejected based on the same rationale as of claim 3.

As in claim 17 Lakhami further discloses wherein the addressing mode field comprise one or more unused bits of the address argument of the command (Lakhani's control bits and address bits corresponds to the claim's address argument. Because the control bits do not contain address bits of memory device such as bits A [22:0] etc..therefore the control bits are unused bits of an address argument as claimed).

As in claim 18, Lakhami disclose a method for operating a non-volatile memory device, the method comprising:

receiving a command that includes an address argument comprising a plurality of address bits and an addressing mode field (Lakhami's paragraphs 73, 76-77, Table A control C1, C2 and address bits A[22:0], E[7:0]), the addressing mode field indicating whether the address argument contains a byte address or a block address (Lakhami's control bits and address bits corresponds to the claim's address argument, Lakhami's paragraphs 73,76-77); and

if the addressing mode field indicates that the address argument contains a byte address, using the address bits to address a byte of data; or

if the addressing mode field indicates that the address argument contains a block address, using

the address bits to address a block of data (Lakhami's paragraphs 73, 76-77 control C1, C2 and address bits A[22:0], E[7:0] provides proper address for a selected address mode).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lakhani et al (US 2003/0126385) and in view of Zer et al (US 2005/0055479).

As in claims 9,10 Lakhani discloses wherein said memory unit is a multi media card (MMC) (claim 9); wherein said memory unit is a secure digital (SD) memory card (claim 10) Lakhani does not expressly disclose the memory is a multi media card or secure digital card. However, Zer's paragraph 6 discloses systems using the removable storage device such as MMC and SD cards. It would have been obvious to one of ordinary skill in the art at the time of invention to use the removable memory cards, for example MMC and SD cards, as suggested by Zer in Lakhani's system thereby further providing secure, light weight, efficient data transferring storage media for various systems such as PDA, cellular telephones (see Zer's paragraphs 6-7).

As in claim 19, Lakhami does not expressly disclose the claim's details associating with the command. However, Zer further disclose wherein the command further comprises a start bit, a transmission bit, a command code, a plurality of CRC checksum bits and an end bit (Zer's paragraph 6 discloses systems using the removable storage device such as MMC and SD cards in which the command Fig 8 includes start bit, transmission bit, command code, CRC bits and end bits as claimed).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the removable memory cards, for example MMC and SD cards, as suggested by Zer in Lakhani's system thereby further providing secure, light weight, efficient data transferring storage media for various systems such as PDA, cellular telephones (see Zer's paragraphs 6-7).

Claims 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lakhani et al (US 2003/0126385) and in view of PCI specification revision 2.2 (herein PCI Specification).

As in claims 20-22 Lakhani does not expressly disclose the claims' detail associating with the addressing mode. However, PCI specification discloses wherein the addressing mode field comprises only a single bit (claim 20, PCI specification's page 202 AD[0]), the address argument contains a byte address when the addressing mode field contains zero (claim 21, PCI specification's page 202, I/O space address mode with AD[0] is zero), the addressing mode field comprises a bit of the address argument (claim 22, PCI specification's page 202, AD[0] comprises a bit of the address argument). It would have been obvious to one of ordinary skill in the art at the time of invention to use the address argument as taught by PCI specification and

thereby further allowing an unused bit AD[0] of the address argument AD[31:0] to be used as an address mode field indicator (see PCI specification page 202).

As in claims 23-24 Lakhani does not expressly disclose the claim's aspect associating with the significant bit of a field such as address argument. However PCI specification discloses an address argument AD [31:0] in which the bits AD[0] represent address mode field, The binary values of AD[0] further indicates two address modes corresponding to accessing data in I/O space and/or memory space. It would have been obvious to one of ordinary skill in the art at the time of invention to use the address argument as taught by PCI specification and thereby further allowing an unused bit AD[0] of the address argument AD[31:0] to be used as an address mode field indicator (see PCI specification page 202). It's further noted that the bit AD[0] can be view as the least significant bit of the address argument accordingly with the little endian notation and can be view as the most significant of the address argument accordingly with the big endian notation as known in the art.

Allowable Subject Matter

Claims 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

Regarding Applicant's remarks at pages 5-10 for the rejections of claims 1-8, and 13-16,17 under 35 U.S.C 102(a) and claims 9-10 under 35 U.S.C 103(a) ,

Applicant argues that "there are no two modes where particular bits.. (i.e the remaining bits in claim 1) provide a byte address in one mode and a block address in the other mode", and somehow LaKhani does not teach the claim's limitation "the remaining bits provide..". Examiner disagrees, Lakhani clearly teaches there are block mode and byte mode wherein in block mode the block address is provided and in byte mode the byte address is provided as recited in the claim (see Lakhani's page 7 table A, paragraph 75 discloses C1,C2 bits being used to determine the first mode, address bits being interpreted as byte address for an operation in a memory device, see paragraph 69; Lakhani's paragraph 76 discloses C1,C2 bits being used to determine the second mode, corresponding to the claim's block mode, in which an operation occurs for data in blocks of memory devices, see paragraph 70).

Lakhani discloses the well known fact that an address field A[22:0] comprise a high order bits such as A[22:A19] which represents a larger block range of addresses and low order bits such as A[4:0] represents a smaller ranges of address and bit A[0] represent the lowest address bit. Examiner contents that this teaching has no bearing whatsoever to the broad limitations being recited in the claim.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

HYUNG S SOUGH
SUPERVISORY PATENT EXAMINER
11/26/07

Notice of References Cited	Application/Control No. 10/766,320	Applicant(s)/Patent Under Reexamination KRYGIER, MARCELO	
	Examiner Duc T. Doan	Art Unit 2188	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
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	F	US-			
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	Q					
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	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	PCI Local Bus Specification Revision 2.2, December 18 1998
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

PCI Local Bus Specification

Revision 2.2

December 18, 1998

Space must return a 0 in bit 0 (see Figure 6-5). Base Address registers that map to I/O Space must return a 1 in bit 0 (see Figure 6-6).

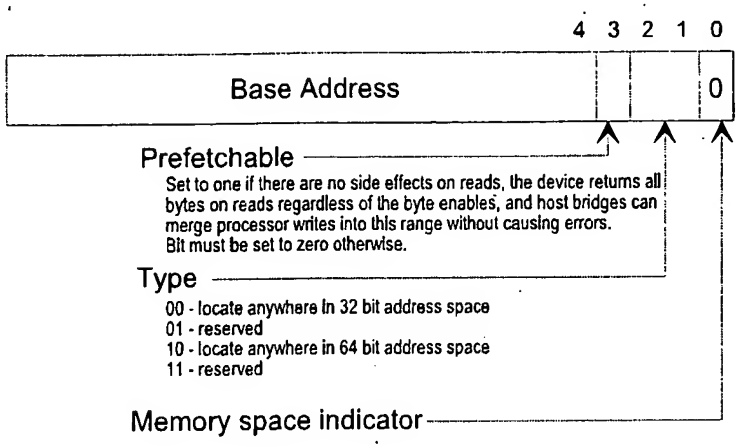

Figure 6-5: Base Address Register for Memory

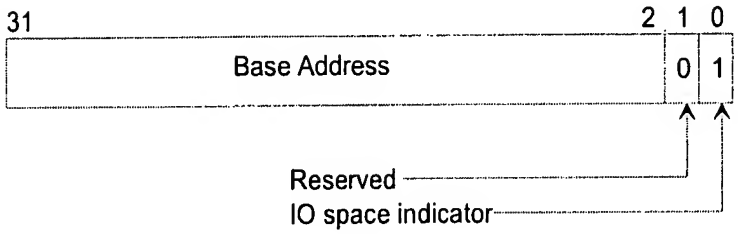

Figure 6-6: Base Address Register for I/O

Base Address registers that map into I/O Space are always 32 bits wide with bit 0 hardwired to a 1. Bit 1 is reserved and must return 0 on reads and the other bits are used to map the device into I/O Space.

Base Address registers that map into Memory Space can be 32 bits or 64 bits wide (to support mapping into a 64-bit address space) with bit 0 hardwired to a 0. For Memory Base Address registers, bits 2 and 1 have an encoded meaning as shown in Table 6-4. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise. A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes (refer to Section 3.2.3.) into this range[45] without causing errors. Bits 0-3 are read-only.

[45] Any device that has a range that behaves like normal memory should mark the range as prefetchable. A linear frame buffer in a graphics device is an example of a range that should be marked prefetchable.